WHAT IS CLAIMED IS:

1. An assembly including a plurality of memory dies within a package, the assembly comprising

a substrate including a number of contact pads formed on a surface thereof;

a first memory die having a first side and a second side, the second side facing the surface of the substrate, the first memory die having at least two memory array portions formed therein, the first side including a plurality of bond pads formed in a center region between the memory array portions, the first memory die further including a redistribution layer that includes re-routing lines that electrically couple the bond pads to re-routed bond pads in a periphery region of the first memory die;

a first plurality of wires electrically coupling re-routed bond pads of the first semiconductor device to contact pads of the substrate;

a second memory die having a first side and a second side, the second side facing the surface of the substrate, the second memory die having at least two memory array portions formed therein, the first side including a plurality of bond pads formed in a center region between the memory array portions, the second memory die further including a redistribution layer that includes re-routing lines that electrically couple the bond pads to re-routed bond pads in a periphery region of the second memory die;

a second plurality of wires electrically coupling re-routed bond pads of the second semiconductor device to contact pads of the substrate, wherein more than half of the second plurality of wires are electrically coupled to a re-routed bond pad that is electrically coupled to one of the first plurality of wires.

2. The assembly of claim 1 wherein the first memory die is identical in structure to the second memory die.

3. The assembly of claim 2 wherein the first and second memory dies comprise dynamic random access memory devices.

4. The assembly of claim 3 wherein the first and second memory dies comprise double-data rate dynamic random access memory devices, each memory device including at least 512 Mb of memory cells.

5. The assembly of claim 4 wherein, for both the first and second memory dies, the bond pads are positioned in a left column and a right column running parallel to a center line through the center region of the device, each bond pad in the left column being located to the left of the center line and each bond pad in the right column being located to the right of the center line, wherein the redistribution layer routes a plurality of bond pads from the right column across the center line to corresponding re-routed bond pads on the left side of the memory die and also routes a plurality of bond pads from the left column across the center line to corresponding re-routed bond pads on the right side of the memory die.

6. The assembly of claim 4 wherein the redistribution layer of each of the first and second memory dies includes a ground plane, the ground plane including a line in the periphery region substantially encircling the bond pads and a plurality of ground lines between some of the re-routing lines.

7. The assembly of claim 6 wherein a plurality of the bond pads comprise data input/output bond pads, wherein the plurality ground lines surround some but not all of the re-routing lines, and wherein the plurality of ground lines run between re-routing lines that are electrically coupled to the data input/output bond pads.

8. The assembly of claim 2 wherein the redistribution layer of the first memory die includes a first set of one or more ground planes and wherein the redistribution layer of the second memory die includes a second set of one or more ground planes.

9. The assembly of claim 8 wherein the first set and the second set each substantially encircles the bond pads on the first memory die and the second memory die, respectively.

10. The assembly of claim 8 wherein the first ground plane and the second ground plane each comprise ground lines adjacent a left side and a right side of a plurality of the re-routing lines.

11. The assembly of claim 2 wherein, for both the first and second memory dies, the re-routed bond pads comprise elongated bond pads extending from an edge of the memory die toward the center region of the memory die, wherein the first plurality of wires are attached to the re-routed bond pads at a portion of the re-routed bond pads nearer the edge and wherein the second plurality of wires are attached to the re-routed bond pads at a portion of the re-routed bond pad nearer the center region.

12. The assembly of claim 2 wherein the redistribution layer of the first and second memory dies comprise a multi-layer structure.

13. The assembly of claim 12 wherein redistribution layer comprises:

a titanium layer;

a copper layer formed on the titanium layer;

a nickel layer formed on the copper layer; and

a gold layer formed on the nickel layer.

14. The assembly of claim 1 and further comprising a spacer disposed between the first memory die and the second memory die.

15. The assembly of claim 14 wherein the first memory die and the second memory die are both formed on a silicon substrate and wherein the spacer comprises a silicon spacer.

16. The assembly of claim 1 wherein the substrate includes at least one wiring layer formed inside the substrate, the wiring layer electrically coupling the contact pads to conductive balls on a second surface of the substrate.

17. A semiconductor device comprising:

an integrated circuit chip including active circuitry formed in a semiconductor substrate and bond pads electrically coupled to components of the active circuitry;

a protective layer overlying the integrated circuit chip and so that bond pads are exposed, the bond pads being positioned on a left side and a right side of a first line in an interior region of the integrated circuit chip; and

a redistribution layer formed over the protective layer, the redistribution layer including a plurality of re-route lines each electrically coupling a bond pad in the interior region to a corresponding re-routed bond pad in a periphery region of the integrated circuit chip, wherein the redistribution layer routes a plurality of bond pads from the right side across the first line to corresponding re-routed bond pads on the left side of the integrated circuit chip and also routes a plurality of bond pads from the left side across the first line to corresponding re-routed bond pads on the right side of the integrated circuit chip.

18. The semiconductor device of claim 17 wherein the integrated circuit comprises a dynamic random access memory (DRAM).

19. The semiconductor device of claim 17 wherein the protective layer is formed of polyimide.

20. The semiconductor device of claim 17 wherein the bond pads are formed in exactly two columns running down the center region of the protective layer, each column including at least 30 bond pads.

21. The semiconductor device of claim 17 wherein the redistribution layer comprises a multi-layer structure.

22. The semiconductor device of claim 21 wherein redistribution layer comprises:

a titanium layer formed on the protective layer;

a copper layer formed on the titanium layer;

a nickel layer formed on the copper layer; and

a gold layer formed on the nickel layer.

23. The semiconductor device of claim 17 wherein the redistribution layer includes a ground plane.

24. The semiconductor device of claim 23 wherein the ground plane includes a conductive line that substantially encircles the re-routed the bond pads.

25. The semiconductor device of claim 24 wherein the ground plane further includes ground lines disposed between ones of the re-route lines that are electrically coupled to data lines of the integrated circuit.

26. A semiconductor device comprising:

an integrated circuit chip including active circuitry formed in a semiconductor substrate and bond pads electrically coupled to components of the active circuitry;

a protective layer overlying the integrated circuit chip and exposing the bond pads, the bond pads being positioned in the interior region of the integrated circuit chip;

a redistribution layer formed over the protective layer, the redistribution layer having re-routing lines, the re-routing lines electrically coupling the bond pads located in the interior region of the semiconductor die to re-routed bond pads in a periphery region of the integrated circuit chip; and

a ground plane formed over the protective layer, the ground plane including a line substantially surrounding the re-routed bond pads and a plurality of ground lines between some of the re-routing lines.

27. The semiconductor device of claim 26 wherein the plurality of ground lines are between some but not all of the re-routing lines.

28. The semiconductor device of claim 26 wherein the integrated circuit chip comprises a DRAM.

29. The semiconductor device of claim 28 wherein the integrated circuit chip comprises a double data rate DRAM and wherein a plurality of the bond pads comprise data input/output bond pads.

30. The semiconductor device of claim 29 wherein the plurality of ground lines are between some but not all of the re-routing lines, and wherein the plurality of ground lines are between re-route lines that are coupled to the data input/output bond pads.

31. The semiconductor device of claim 29 wherein the bond pads are positioned in a left column and a right column that each run parallel to a center line in the interior region of the integrated circuit chip, each bond pad in the left column being located to the left of the center line and each bond pad in the right column being located to the right of the center line, and wherein at least some of the re-routing lines electrically couple a plurality of bond pads from the right column across the center line to corresponding re-routed bond pads on the left side of the integrated circuit chip and some others of the re-routing lines electrically couple bond pads from the left column across the center line to corresponding re-routed bond pads on the right side of the integrated circuit chip.

32. The semiconductor device of claim 26 wherein redistribution layer comprises:

a titanium layer formed on the protective layer;

a copper layer formed on the titanium layer;

a nickel layer formed on the copper layer; and

a gold layer formed on the nickel layer.

33. A stacked-die assembly comprising:

a substrate;

a first die located above the substrate, the first die having a first side and a second side facing the substrate, the first side of the first die having a redistribution layer formed thereon, the redistribution layer including re-routing lines to re-route a plurality of bond pads from an interior region to re-routed bond pads in a periphery region, and the first side of the first die having a ground plane substantially encircling the periphery region and at least some of the re-routing lines; and

a second die located above the first die, the second die having a first side and a second side facing the first die, the first side of the second die having a redistribution layer formed thereon, the redistribution layer including re-routing lines to re-route a plurality of bond pads from an interior region to re-routed bond pads in a periphery region, and the first side of the first die having a ground plane substantially encircling the periphery region and at least some of the re-routing lines.

34. The stacked-die assembly of claim 33 wherein the first die and the second die comprise DRAM semiconductor devices.

35. The stacked-die assembly of claim 33, wherein redistribution layers of both the first die and the second die comprise:

a titanium layer formed on a protective layer of the die;

a copper layer formed on the titanium layer;

a nickel layer formed on the copper layer; and

a gold layer formed on the nickel layer.

36. The stacked-die assembly of claim 33 wherein the ground plane comprises a plurality of ground lines between data lines.

37. The stacked-die assembly of claim 33 wherein the redistribution layer of at least one of the first die and the second die re-routes bond pads from the left side or the right side to the other side.

38. The stacked-die assembly of claim 33 further comprising one or more additional dies stacked on the second die.

39. The stacked-die assembly of claim 33 wherein the size of the second die is such that the second die does not cover the re-routed bond pads of the first die.

40. The stacked-die assembly of claim 33 further comprising a spacer positioned between the first die and the second die.

41. A stacked-die assembly comprising:

a substrate;

a first die located above the substrate, the first die having a top side and a bottom side, the top side having bond pads formed in the interior region of the first die and having a redistribution layer re-routing bond pads from the interior region to re-routed bond pads in a periphery region of the first die, and the second side of the first die facing the substrate; and

a second die located above the first die, the second die having a first side and a second side, the first side of the second die having bond pads in the interior region of the second die and having a redistribution layer re-routing bond pads from the interior region to re-routed bond pads in a periphery region of the second die, and the second side of the second die facing the substrate;

wherein at least one bond pad of at least one of the first die and the second die are routed from the left side or the right side to the other.

42. The stacked-die assembly of claim 41 wherein the first die and the second die comprise DRAM semiconductor devices.

43. The stacked-die assembly of claim 41 wherein redistribution layers of both the first die and the second die comprise:

a titanium layer formed on a protective layer of the die;

a copper layer formed on the titanium layer;

a nickel layer formed on the copper layer; and

a gold layer formed on the nickel layer.

44. The stacked-die assembly of claim 41 wherein redistribution layers of both the first die and the second die comprise a ground plane that includes a plurality of ground lines disposed between data re-routing lines.

45. The stacked-die assembly of claim 41 further comprising one or more additional dies stacked on the second die.

46. The stacked-die assembly of claim 41 wherein the size of the second die is such that the second die does not cover the re-routed bond pads of the first die.

47. The stacked-die assembly of claim 41 further comprising a spacer positioned between the first die and the second die.

48. A stacked-die assembly comprising:

a substrate including contact pads located adjacent a periphery of a top surface of the substrate, each of the contact pads being electrically coupled to conductors on a bottom surface of the substrate;

a plurality of identical dies stacked vertically over the substrate, each of the dies having a redistribution layer formed on a top side, the redistribution layer having a plurality of conductive lines re-routing a plurality of bond pads located in columns in an interior region to re-routed bond pads in a periphery region, the redistribution layer having a ground plane comprising grounded lines separating the conductive lines corresponding to data lines;

for each adjacent pair of dies, a spacer disposed between the two dies; and

a plurality of bond wires, each bond wire electrically coupling one of the re-routed bond pads to a corresponding contact pad on the substrate.

49. The stacked-die assembly of claim 48 wherein the dies comprise DRAM semiconductor dies.

50. The stacked-die assembly of claim 48 wherein the ground plane further comprises a ground line substantially encircling the bond pads.

51. The stacked-die assembly of claim 48 wherein the redistribution layer re-routes a plurality of bond pads from the left side to the right side and a plurality of bond pads from the right side to the left side.

52. The stacked-die assembly of claim 48 wherein the re-routed pads comprise elongated pads and wherein the location of the bond wires on the rerouted pad is related to the distance of the die from the substrate.

53. A method of forming a stacked-die assembly, the method comprising:

providing a substrate with contacts formed on a top surface;

placing a bottom side of a first die over the top surface of the substrate, the first die having a top side with a redistribution layer that comprises conductive lines that redistribute bond pads located on a right side and a left side of a first gap in an interior region to corresponding re-routed bond pads in a periphery region;

placing a spacer over the first die;

placing a bottom side of a second die over the spacer, the second die having a first side with a redistribution layer that comprises conductive lines that redistribute bond pads located on a right side and a left side of a first gap in an interior region to corresponding re-routed bond pads in a periphery region; and

electrically coupling wire leads from the re-routed bond pads of the first die and the second die to the contacts.

54. The method of claim 53 wherein the step of electrically coupling is performed by wire bonding.

55. The method of claim 54 wherein the wire bonding is performed further to the interior of the second die relative to the bonding of the first die.

56. The method of claim 53 wherein the first die is identical in structure to the second die.

57. The method of claim 56 wherein the first and second dies comprise dynamic random access memory devices.

58. The method of claim 57 wherein the first and second dies comprise double-data rate dynamic random access memory devices, each memory device including at least 512 Mb of memory cells.

59. The method of claim 56 wherein, for both the first and second dies, the bond pads are positioned in a left column and a right column running parallel to a center line through the interior region, each bond pad in the left column being located to the left of the center line and each bond pad in the right column being located to the right of the center line, wherein the redistribution layer routes a plurality of bond pads from the right column across the center line to corresponding re-routed bond pads on the left side of the semiconductor device and also routes a plurality of bond pads from the left column across the center line to corresponding re-routed bond pads on the right side of the semiconductor device.

60. The method of claim 56 wherein the redistribution layer of each of first and second dies includes a ground plane, the ground plane including a line substantially encircling the re-routed bond pads and a plurality ground lines that surround some of the re-routing lines.

61. The method of claim 60 wherein a plurality of the bond pads comprise data input/output bond pads, wherein the plurality ground lines surround some but not all of the re-routing lines, and wherein the plurality ground lines surround re-routing lines that are electrically coupled to the data input/output bond pads.

62. The method of claim 56 wherein the redistribution layer of the first die includes a first ground plane and wherein the redistribution layer of the second die includes a second ground plane.

63. The method of claim 62 wherein the first ground plane and the second ground plane each comprise a line substantially encircling the re-routed bond pads.

64. The method of claim 62 wherein the first ground plane and the second ground plane each comprise ground lines adjacent a left side and a right side of a plurality of the conductive lines.

65. The method of claim 53 wherein, for both the first and second dies, the re-routed bond pads comprise elongated bond pads extending from an edge of the die toward the interior region of the die, wherein electrically coupling wire leads comprises:

for the first die, attaching wires to the re-routed bond pads at a portion of the re-routed bond pads nearer the edge of the first die; and

for the second die, attaching wires to the re-routed bond pads at a portion of the re-routed bond pad nearer the interior region of the second die.

66. The method of claim 53 wherein the redistribution layer of the first and second dies comprise a multi-layer structure.

67. The method of claim 66 wherein redistribution layer comprises:

a titanium layer;

a copper layer formed on the titanium layer;

a nickel layer formed on the copper layer; and

a gold layer formed on the nickel layer.

68. The method of claim 53 wherein the first die and the second die are both formed on a silicon substrate and wherein the spacer comprises a silicon spacer.

69. The method of claim 53 wherein the substrate includes at least one wiring layer formed inside the substrate, the wiring layer electrically coupling the contact pads to conductive balls on a second surface of the substrate.

70. The method of claim 53 wherein placing the first die over the substrate comprises adhering the first die to the substrate with tape.

71. The method of claim 53 wherein placing the first die over the substrate comprises printing an adhesive over the substrate and placing the first die in the adhesive.

72. The method of claim 53 wherein electrically coupling wire leads from the re-routed bond pads of the first die and the second die to contacts formed in the substrate comprises electrically coupling wire leads from the re-routed bond pads of the first die before placing a spacer over the first die and electrically coupling wire leads from the re-routed bond pads of the second die after placing the second die over the spacer.

73. A method of forming a stacked-die assembly, the method comprising:

providing a substrate with contacts formed on a top surface;

placing a bottom side of a first die over the top surface of the substrate, the first die having a top side with a redistribution layer that comprises conductive lines that redistribute bond pads located on a right side and a left side of a first gap in an interior region to corresponding re-routed bond pads in a periphery region;

placing a bottom side of a second die over the spacer, the second die having a first side with a redistribution layer that comprises conductive lines that redistribute bond pads located on a right side and a left side of a first gap in an interior region to corresponding re-routed bond pads in a periphery region; and

electrically coupling wire leads from the re-routed bond pads of the first die and the second die to the contacts

wherein the first die is a different size than the second die and the second die is positioned on the first die such that the re-routed bond pads of the first die are not covered by the second die.

74. The method of claim 73 wherein the step of electrically coupling is performed by wire bonding.

75. The method of claim 74 wherein the wire bonding is performed further to the interior of the second die relative to the bonding of the first die.

76. The method of claim 74 wherein at least one of the first and second dies comprise dynamic random access memory devices.

77. The method of claim 76 wherein at least one of the first and second dies comprise double-data rate dynamic random access memory devices, each memory device including at least 512 Mb of memory cells.

78. The method of claim 73 wherein, for both the first and second dies, the bond pads are positioned in a left column and a right column running parallel to a center line through the interior region, each bond pad in the left column being located to the left of the center line and each bond pad in the right column being located to the right of the center line, wherein the redistribution layer routes a plurality of bond pads from the right column across the center line to corresponding re-routed bond pads on the left side of the semiconductor device and also routes a plurality of bond pads from the left column across the center line to corresponding re-routed bond pads on the right side of the semiconductor device.

79. The method of claim 73 wherein the redistribution layer of each of first and second dies includes a ground plane, the ground plane including a line substantially encircling the re-routed bond pads and a plurality ground lines that surround some of the re-routing lines.

80. The method of claim 79 wherein a plurality of the bond pads comprise data input/output bond pads, wherein the plurality ground lines surround some but not all of the re-routing lines, and wherein the plurality ground lines surround re-routing lines that are electrically coupled to the data input/output bond pads.

81. The method of claim 73 wherein the redistribution layer of the first die includes a first ground plane and wherein the redistribution layer of the second die includes a second ground plane.

82. The method of claim 81 wherein the first ground plane and the second ground plane each comprise a line substantially encircling the re-routed bond pads.

83. The method of claim 82 wherein the first ground plane and the second ground plane each comprise ground lines adjacent a left side and a right side of a plurality of the conductive lines.

84. The method of claim 73 wherein, for both the first and second dies, the re-routed bond pads comprise elongated bond pads extending from an edge of the die toward the interior region of the die, wherein electrically coupling wire leads comprises:

for the first die, attaching wires to the re-routed bond pads at a portion of the re-routed bond pads nearer the edge of the first die; and

for the second die, attaching wires to the re-routed bond pads at a portion of the re-routed bond pad nearer the interior region of the second die.

85. The method of claim 73 wherein the redistribution layer of the first and second dies comprise a multi-layer structure.

86. The method of claim 86 wherein redistribution layer comprises:

a titanium layer;

a copper layer formed on the titanium layer;

a nickel layer formed on the copper layer; and

a gold layer formed on the nickel layer.

87. The method of claim 73 wherein the first die and the second die are both formed on a silicon substrate and wherein the spacer comprises a silicon spacer.

88. The method of claim 73 wherein the substrate includes at least one wiring layer formed inside the substrate, the wiring layer electrically coupling the contact pads to conductive balls on a second surface of the substrate.

89. The method of claim 73 wherein placing the first die over the substrate comprises adhering the first die to the substrate with tape.

90. The method of claim 73 wherein placing the first die over the substrate comprises printing an adhesive over the substrate and placing the first die in the adhesive.

91. The method of claim 73 wherein electrically coupling wire leads from the re-routed bond pads of the first die and the second die to contacts formed in the substrate comprises electrically coupling wire leads from the re-routed bond pads of the first die before placing a spacer over the first die and electrically coupling wire leads from the re-routed bond pads of the second die after placing the second die over the spacer.